REMARKS

Applicants respectfully request reconsideration of this application.

Amendments to the specification either update a reference to a parent application or correct typographical errors. Applicants submit that no new matter has been added.

Claims 1-3, 7-10, 14-19 and 21-22 have been amended. Claims 23-25 have been added. Amendments to the claims are made only to place the claims in what Applicants consider to be better form and not in response to the rejections. Applicants do not believe any amendment is needed to comply with any requirement of patentability.

Drawings

Applicants thank the Examiner for approving the drawings previously submitted.

Rejections under 35 U.S.C. §102

Examiner rejected Claims 1, 7, 9, 14, 16, and 21 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,724,084 to *Hikita* et al. Applicants respectfully submit that *Hikita* does not anticipate the present claims.

Applicants have amended independent claim 1 to clarify that the wafer bonding method is to form integrated chips. *Hikita* is directed towards chip-on-chip structures and flip-chip-bonded structures in which a chip is bonded to a printed circuit board. (*Hikita*, Field of Invention). Therefore, *Hikita* is directed towards bonding at a different stage of processing and fails to disclose or suggest the limitations of claim 1.

For example, claim 1 includes the limitation "selectively depositing a plurality of metallic lines into interlevel dielectrics (ILDs) on opposing surfaces of adjacent wafers." *Hikita* does not teach or disclose depositing metallic lines into interlevel dielectrics (ILDs).

Rather, *Hikita* discloses depositing metal bumps on an electrode 83 covered by a passivation film 84 covered by a seed layer 85. (See, *Hikita*, Figures 1C-1E and col. 10, lines 1-3, 14-18 and 24-30). Specifically, *Hikita* discloses that "the bump formed on the Al electrode 83 is denoted by a reference numeral 88". (*Hikita*, col. 10, lines 24-31).

Examiner suggests that the bump 88 is the metallic lines of claims 1, 9 and 16. (Office Action, dated April 12, 2005, p. 2). However, the bump 88 is formed on a seed layer 85 (*Hikita*, col. 10, lines 14, Fig. 1C-1E and Fig. 4B) and not into an interlevel dielectric on a surface of a wafer. Therefore, *Hikita* does not teach or suggest a wafer bonding method to form integrated chips and does not teach or suggest "selectively depositing a plurality of metallic lines into interlevel dielectrics (ILDs) on opposing surfaces of adjacent wafers."

Therefore, *Hikita* fails to teach or suggest all of the limitations in claim 1. Independent claims 9 and 16 include a similar limitation. Accordingly, *Hikita* fails to anticipate independent claims 1, 9 and 16. Claims 7, 14 and 21 depend from the foregoing independent claims. Therefore, *Hikita* fails to anticipate claims 7, 14 and 21 for at least the reasons discussed above. Withdrawal of the rejection is respectfully requested.

Rejections under 35 U.S.C. §103

Examiner rejected claims 2, 10, 17, and 18 under 35 U.S.C. § 103(a) as being unpatentable over *Hikita* in view of U.S. Patent No. 6,340,608 to *Chooi* et al.

As discussed above, *Hikita* fails to teach or suggest selectively depositing a plurality of metallic lines into interlevel dielectrics (ILDs) on opposing surfaces of adjacent wafers. Applicants respectfully submit that *Chooi* also fails to teach or suggest selectively depositing a plurality of metallic lines into interlevel dielectrics (ILDs) on opposing surfaces of adjacent wafers. Accordingly, neither *Hikita*, nor *Chooi*, nor the combination thereof teach or suggest the limitations of independent claims 1, 9 and 16, from which claims 2, 10, 17, and 18 depend, respectively. Accordingly, Applicants respectfully request withdrawal of the rejection of claims 2, 10, 17, and 18 under 35 U.S.C. §103(a).

Allowable Subject Matter

Examiner indicated that, regarding dependent claim 3, the prior art fails to teach a dielectric recess for ensuring that the metal lines on one wafer contact the metal lines on the other wafer. (Office Action, dated April 12, 2005, p. 4). Applicants have herein added new claim 23 based on the limitations of claim 3. Specifically, new claim 23 includes the limitation "the plurality of metallic lines are surrounded by a dielectric recess to ensure that the metallic lines on the first wafer contact the metallic lines on the second wafer." Applicants respectfully submit that claim 23 is in condition for allowance.

Examiner also indicated that the prior art does not suggest applying a barrier to an outer edge of a bonded wafer having a plurality of dice. (Office Action, dated April 12, 2005, p. 4). Applicants have herein added new claim 24 directed towards such a barrier. Specifically, claim 24 includes the limitation "barrier line on an outer edge of a surface of a first wafer having a plurality of die." Applicants respectfully submit that claim 24 is in condition for allowance.

Finally, Examiner indicated that the prior art generally teaches the usage of a single guard ring deposited on the perimeter of the die, but that there is no suggestion or motivation in the prior art for providing a barrier in the shape of concentric rings. (Office Action, dated April 12, 2005, p. 5). Applicants have herein added new claim 25 directed such a barrier. Specifically, claim 25 includes the limitation "set of concentric guard rings on the perimeter of a first die." Applicants respectfully submit that claim 25 is in condition for allowance.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance.

Pursuant to 37 C.F.R. 1.136(a)(3), Applicants hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 02-2666.

Respectfully submitted,
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